



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
-----------------	-------------	----------------------	---------------------	------------------

10/523,984

02/08/2005

Jin-Koo Chung

21C.0324

1578

23413 7590 03/17/2008
CANTOR COLBURN, LLP
20 Church Street
22nd Floor
Hartford, CT 06103

EXAMINER

MACCHIAROLO, PETER J

ART UNIT

PAPER NUMBER

2879

MAIL DATE

DELIVERY MODE

03/17/2008

PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 10/523,984	Applicant(s) CHUNG ET AL.	
	Examiner PETER J. MACCHIAROLO	Art Unit 2879	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 28 January 2008.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-26 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-26 is/are rejected.
- 7) ☒ Claim(s) 12-14 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Continued Examination

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application on 01/28/2008. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.14. Applicant's submission filed on 01/28/2008 has been entered. However, pending claims 1-26 are not allowable as explained below. An action on the RCE follows.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated Yamada et al (USPN 6833668; “Yamada”)

Regarding claim 1, Yamada discloses at least in figures 2c-3b a display device comprising: a substrate (fig. 3a; 1) having a first region (inside enclosed by 12) and a second region (area outside of 12) surrounding the first region; a plurality of first electrodes (4) disposed in the first region (12); an insulation member (fig. 2c; not labeled) arranged in the first region (12) and having a plurality of openings (not labeled, shown in fig. 3b) that exposes a portion corresponding to each of the first electrodes (4); light emitting patterns (5) disposed directly on

the first electrodes (4), the light emitting patterns (5) filling up the openings (not labeled), respectively; and a single second electrode (6) formed on substantially an entire face of the substrate, the single second electrode (6) disposed on the light emitting patterns (60).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-7, 10, 15, 17-21, 25 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over previously cited Nakanishi et al (US PG PUB 20040070808: “Nakanishi”) in view of Yudasaka (USPN 6380672: “Yudasaka”).

Regarding claim 1, Nakanishi discloses at least in figures 2, 4, and 5 a display device comprising: a substrate (20) having a first region (inside area of 3 best seen at fig. 8) and a second region (outside region of 3 best seen at fig. 8) surrounding the first region (inside area of 3); a plurality of first electrodes (23) disposed in the first region (inside area of 3); an insulation member (221b) arranged in the first region (inside area of 3) and having a plurality of openings (not labeled, shown as rectangular openings in fig. 5a) that exposes a portion (26) corresponding to each of the first electrodes (23); light emitting patterns (60) disposed directly on the first electrodes (23), the light emitting patterns (60) filling up the openings (not labeled), respectively; and a single second electrode (50) disposed on the light emitting patterns (60).

Nakanishi is silent to the single second electrode being disposed directly on the insulation member.

However, Yudasaka teaches in at least col. 2, ll. 4-12 and col. 3, ll. 1-9 that forming a single second electrode (op) substantially an entire face of the substrate and disposed directly on the insulation member (bank 61 and 62) allows for simple and reliable construction and eliminates the need for any extra film which may increase the thickness of the overall device.

Therefore, in view of the above discussion, it would have been obvious to one having ordinary skill in the art at the time the invention was made to construct the device of Nakanishi with one single second of Yudasaka to allow for a simpler, and therefore less expensive slim light emitting device.

Regarding claim 2, Nakanishi discloses at least in figure 3 and paragraphs 74-76 a plurality of dummy light emitting patterns (functional layer 110 in region 5) formed in the second region (outside area of 3) of the substrate (20).

Regarding claim 3, Nakanishi discloses at least in figure 2 the openings (not labeled) have a rectangular shape that has a pair of long sides (shown in Y axis direction in figure 2) and a pair of short sides (shown in X axis direction in figure 2), and the openings (not labeled) are arranged in a matrix shape along a first direction that is substantially parallel with the long sides and a second direction that is substantially parallel with the short sides in the first region (inside area of 3).

Regarding claim 4, Nakanishi discloses at least in figures 2, 3, and 5 a side face (23a) of the insulation member is extended from the first region (inside area of 3) to the second region (outside area of 3) in the first direction and an extending length of the insulation member is equal to or less than a width formed between the openings (not labeled). The Examiner notes that no bounds have been given to “an external length,” (i.e. a length from the interface of the first and second region to the edge of the insulation member) therefore the Examiner has interpreted the bounds to be any arbitrary point at a distance less than a width formed between the openings.

Regarding claim 5, Nakanishi discloses at least in figures 3, 5, and 2 a side face of the insulation member is extended from the first region (inside area of 3) to the second region (outside area of 3) in the second direction, and an extending length is equal to or less than a width formed between the openings (not labeled). The Examiner notes that no bounds have been given to “an external length,” (i.e. a length from the interface of the first and second region to the edge of the insulation member) therefore the Examiner has interpreted the bounds to be any arbitrary point at a distance less than a width formed between the openings.

Regarding claim 6, Nakanishi discloses at least in figures 5a and 5b the openings (not labeled) are essentially disposed on the center of the first electrodes (23), respectively.

Regarding claim 7, Nakanishi discloses at least in figures 5a and 5b and paragraph 80 that each of the light emitting patterns (110) includes a hole injection layer (70) and a light emitting layer (60), and the light emitting layer (110) is formed on the hole injection layer (70).

Regarding claim 10, Nakanishi discloses at least in paragraph 74 the insulation member includes an organic material, an inorganic material or a photoresist material.

Regarding claim 15, Nakanishi discloses at least in figures 2, 3, and 5 a display device comprising a substrate (20) having a first region (inside area of 3 best seen at fig. 8) and a second region (outside area of 3 best seen at fig. 8) surrounding the first region (inside area of 3 best seen at fig. 8); a plurality of first electrodes (23) disposed in the first region (inside area of 3 best seen at fig. 8); an insulation film (221b), formed on the substrate to cover the first electrodes (23), having a plurality of first (inside, not labeled but best seen at fig. 2) and second (outside, not labeled but in area 5 of fig. 3) openings, the first openings exposing a portion corresponding to each of the first electrodes (23), the second openings disposed in the second region (outside area of 3 best seen at fig. 8); light emitting patterns (110) disposed on the first electrodes (23), the light emitting patterns (110) filling up the first openings, respectively; and a second electrode (50) disposed on the light emitting patterns (110).

Nakanishi is silent to the single second electrode being disposed directly on the insulation member.

However, as discussed in the rejection of claim 1, Yudasaka teaches in at least col. 2, ll. 4-12 and col. 3, ll. 1-9 that forming a single second electrode (op) substantially an entire face of the substrate and disposed directly on the insulation member (bank 61 and 62) allows for simple and reliable construction and eliminates the need for any extra film which may increase the thickness of the overall device.

Therefore, in view of the above discussion, it would have been obvious to one having ordinary skill in the art at the time the invention was made to construct the device of Nakanishi with one single second of Yudasaka to allow for a simpler, and therefore less expensive slim light emitting device.

Regarding claim 16, Nakanishi discloses at least in figures 3 and 5 a first width of the first openings is equal to or less than a second width of the second openings.

Regarding claim 17, Nakanishi discloses at least in figure 3 and paragraphs 74-76 a plurality of dummy light emitting patterns (functional layer 110 in region 5) are formed on the substrate corresponding to each of the second openings.

Regarding claim 18, Nakanishi discloses at least in figures 7a-7d a method of manufacturing a display device comprising: forming a plurality of first electrodes (23) in a first region (inside area of 3 best seen at fig. 8) formed on a substrate (20); forming an insulation member (221b) on the first region, wherein the insulation member has a plurality of openings (not labeled) each exposing a portion (not labeled) corresponding to each of the first electrodes; forming light emitting patterns (110) on the first electrodes, respectively; and forming a second electrode (50) in the first region to cover the light emitting patterns.

Nakanishi is silent to the single second electrode being disposed directly on the insulation member.

However, as discussed in the rejection of claim 1, Yudasaka teaches in at least col. 2, ll. 4-12 and col. 3, ll. 1-9 that forming a single second electrode (op) substantially an entire face of the substrate and disposed directly on the insulation member (bank 61 and 62) allows for simple and reliable construction and eliminates the need for any extra film which may increase the thickness of the overall device.

Therefore, in view of the above discussion, it would have been obvious to one having ordinary skill in the art at the time the invention was made to construct the device of Nakanishi with one single second of Yudasaka to allow for a simpler, and therefore less expensive slim light emitting device.

Regarding claims 19 and 20, Nakanishi discloses at least in figures 7a-7d a conductive layer (23) including a transparent conductive material (ITO, see for example paragraph 79) is formed on the substrate (20) and the conductive material is patterned to form the first electrodes (23) in the first region.

Regarding claim 21, Nakanishi discloses at least in figures 2, 3, 5, and 7a-7d the openings (not labeled) have a rectangular shape that has a pair of long sides (shown in Y axis direction in figure 2) and a pair of short sides (shown in X axis direction in figure 2), and the openings (not labeled) are arranged in a matrix shape along a first direction that is substantially parallel with the long sides and a second direction that is substantially parallel with the short sides in the first region (inside area of 3).

Regarding claim 25, Nakanishi discloses at least in figures 2, 3, 5, and 7a-7d and paragraph 129, a hole injection material (70) as a droplet shape is dropped on the first electrode (23) so as to form a hole injection layer of the light emitting patterns (110) and a light emitting material (60) as a droplet shape is dropped on the hole injection layer so as to form a light emitting layer of the light emitting patterns.

Regarding claim 26, Nakanishi discloses at least in figures 2, 3, 5, and 7a-7d a plurality of dummy light emitting patterns (functional layers in region 5 shown in fig. 3) are disposed in the second region.

The Examiner notes that the limitation, “to adjust a speed of drying the light emitting patterns” is an intended use type limitation. A recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. See *In re Casey*, 152 USPQ 235 (CCPA 1967) and *In re Otto*, 136 USPQ 458, 459 (CCPA 1963).

Claims 8 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakanishi and Yudasaka in further view of Nagayama et al (USPN 6137220: “Nagayama”).

Regarding claim 8, Nakanishi and Yudasaka are silent to the exact angle of the inside wall of the openings.

However, Nagayama teaches at least in figure 2a, the abstract, and col. 5 lines 45-57 that an inside wall of the openings has an angle about 30° to 165° with respect to the first electrodes

formed on the substrate, and this configuration allows organic EL material deposition method that prevents any ingress of moisture into the device.

Therefore, in view of the above discussion, it would have been obvious to one having ordinary skill in the art at the time the invention was made to construct the device of Nakanishi and Yudasaka with the inside wall of the openings has an angle about 30° to 165° to allow for an organic EL material deposition method which prevents any ingress of moisture into the device.

Regarding claim 9, Nakanishi discloses at least in paragraphs 79 the first electrodes (23) include a transparent conductive material (ITO), but is silent to the second electrode (50) including an opaque conductive material.

However, Nagayama teaches at least in col. 5, ll. 57-64 that using an opaque second electrode (made of aluminum) and a transparent first electrode (ITO) is a known electrode configuration. One would be motivated to this configuration to reflect light emitted from the EL layer off of the opaque electrode to exit the transparent electrode to improve light emitting efficiency.

Therefore, in view of the above discussion, it would have been obvious to one having ordinary skill in the art at the time the invention was made to construct the device of Nakanishi and Yudasaka with the first electrode comprising a transparent conductive material and the second electrode including an opaque conductive material to improve light emitting efficiency.

Claims 11-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamada in view of Omura et al (USPN 7053549; “Omura”).

Regarding claim 11, Yamada discloses at least in figures 2c-3b a display device comprising: a substrate (fig. 3a; 1) having a first region (inside enclosed by 12) and a second region (area outside of 12) surrounding the first region; a plurality of first electrodes (4) disposed in the first region (12); an insulation member (fig. 2c; not labeled) arranged in the first region (12) and having a plurality of openings (not labeled, shown in fig. 3b) that exposes a portion corresponding to each of the first electrodes (4); light emitting patterns (5) disposed directly on the first electrodes (4), the light emitting patterns (5) filling up the openings (not labeled), respectively; and a single second electrode (6) formed on substantially an entire face of the substrate, the single second electrode (6) disposed on the light emitting patterns (60).

Yamada is silent to the insulation layer having a groove.

However, Omura teaches in at least in the abstract and in fig. 2 that the insulating layer having a groove reduces the moisture infiltration and increases the lifetime of the lamp.

Therefore, in view of the above discussion, it would have been obvious to one having ordinary skill in the art at the time the invention was made to construct the device of Yamada with the insulating layer having a groove to reduce the moisture infiltration and increases the lifetime of the lamp.

Allowable Subject Matter

Claims 12-14 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

Regarding dependent claim 12, the prior art discloses and teaches a groove being formed in the insulation layer, but fails to teach or suggest the groove is equal to or more than a width of the openings in combination with the remaining limitations of the claims. Claims 13 and 14 would be allowable due to their dependency.

Response to Arguments

Applicant's arguments have been fully considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Peter J Macchiarolo whose telephone number is (571) 272-2375. The examiner can normally be reached on 8:30 - 5:00, M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nimeshkumar Patel can be reached on (571) 272-2475. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Respectfully submitted,

/Peter Macchiarolo/
Patent Examiner, Art Unit 2879
(571) 272-2375